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METHOD AND APPARATUS FOR PROVIDING INTRA-TOOL MONITORING AND CONTROL

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METHOD AND APPARATUS FOR PROVIDING INTRA-TOOL MONITORING AND CONTROL

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention generally relates to semiconductor wafer processing systems and, more particularly, the invention relates to a method and apparatus for monitoring and controlling a plurality of tools within a semiconductor wafer processing system.

Description of the Related Art

[0002] Semiconductor wafer processing systems generally comprise a plurality of distinct tools for performing certain process steps on a wafer (or other form of substrate) to create integrated circuits (or other forms of micro-electronic circuits). Additional tools comprise metrology stations that are used for testing wafers in-between process steps. Generally, the metrology testing is performed to determine the specific accuracy and efficacy of the processes conducted by a particular tool. Depending upon the results of the metrology testing, certain parameters of a particular tool may be adjusted to facilitate improving the function of the tool. However, in such systems the metrology monitoring and control processing does not consider the interactions of multiple tools upon wafer processing. As such, the metrology station measuring wafers at the output of a first tool may determine that the wafers are within tolerances for the particular process conducted in the first tool, while the metrology station measuring wafers at the output of a second tool may find that those wafers are within tolerances for processing from the second tool. However, the combination of the inaccuracies in the first tool and the second tool may cause the processing of the wafer to inaccurately form integrated circuits on the wafer.

[0003] Therefore, there is a need in the art for a method and apparatus that provides intra-tool monitoring and control to more effectively process semiconductor wafers.

SUMMARY OF THE INVENTION

[0004] The present invention generally provides a method and apparatus for performing intra-tool monitoring and control within a multi-step processing system. The method monitors the processing of a workpiece as the workpiece is processed by independently operating processing tools and produces control parameters for the various independently operating processing tools to optimize the processing of the workpiece.

[0005] More specifically, the invention provides one or more metrology stations that can be used between processing steps of each tool in a plurality of tools such that measurements can be made on wafers as they are passed from one tool to another providing intra-tool monitoring. The data collected by the metrology station is coupled to a metrology data analyzer, which determines whether any of the plurality of wafer processing tools should be adjusted to improve the processing of the overall wafer. As such, the output of the metrology data analyzer provides control parameters to process controllers connected to each of the tools within the semiconductor wafer processing system. Consequently, the metrology station(s) and the metrology data analyzer provide both feed-forward and feedback data to control the tools based upon information that is gathered within the metrology station at specific instances in time or after particular process steps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] So that the manner in which the above recited features of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0007] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0008] FIG. 1 is a block diagram of a semiconductor wafer processing system utilizing the present invention;

[0009] FIG. 2 is a flow diagram of a process in accordance with the present invention;

[0010] FIG. 3 depicts a flow diagram of a process for manufacturing a copper interconnect in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0011] FIG. 1 depicts a block diagram of a semiconductor wafer processing system 100 comprising a plurality of tools 102, 104, 106 for processing semiconductor wafers in a serial manner, a plurality of processor controllers 108, 110, 112, one or more metrology stations 114 and a metrology data analyzer 116. Each process controller 108, 110, and 112 is respectively coupled to a tool 102, 104, and 106. In FIG. 1 (and FIG. 3 below) the thick arrows represent wafer movement and the thin arrows represent electrical signals or data signals. To process a wafer, a wafer is illustratively placed in tool A 102 and processed, then passed to tool B 104 and then to tool C 106. The completed wafer containing certain integrated circuits or intermediate structures for producing integrated circuits is output from tool C 106. Generally, the tools are independently operating tools such as etch chambers, electrochemical plating (ECP) cells, chemical-mechanical polishing (CMP) tools, and deposition chambers such as physical vapor deposition (PVD) and chemical vapor deposition (CVD).

[0012] Those skilled in the art will realize that the sequential ordering of the three tools shown in FIG. 1 is only illustrative of the invention and wafers during processing may be passed in both directions within the semiconductor wafer processing system or additional tools may be used within the system. Furthermore, the illustrative embodiments of the invention are described herein with respect to manufacturing integrated circuits on a semiconductor wafer. However, the invention is useful many other manufacturing environments where precise control of multi-step processing is required. Such manufacturing may include component machining, microelectronics

fabrication, flat panel display fabrication, and the like. As such, the "wafer" in the following descriptions is one embodiment of a workpiece that is sequentially processed in various process steps to fabricate a product.

[0013] During intermediate process steps, wafers are removed from processing and placed in the metrology station(s) 114. Within the metrology station or stations 114, the wafers are measured to identify whether or not the layers, structures or features are within certain parameters. The wafer selected for the metrology station(s) may be certain types of test wafers such as blanket wafers or patterned wafers that are used for identifying certain anomalies that may occur as a result of processing by one or more of the tools. Alternatively, the wafers being tested may be selected from actual process wafers. Every process wafer or a subset may be tested.

[0014] The data from the metrology station(s) 114 is coupled to the metrology data analyzer 116. The metrology data is analyzed to determine if the tools 102, 104, 106 need to be adjusted to better process the wafers. The control signals from the metrology data analyzer 116 are coupled to the process controllers 108, 110, 112 for each tool 102, 104, 106 such that the metrology data analyzer 116 can use data collected from each tool to either feed-forward or feedback control signals to improve processing of the wafers.

[0015] Consequently, metrology station(s) 114 may find that tool A 102 is not correctly processing the wafer such that the metrology data analyzer 116 will feedback a signal to the process controller 108 for tool A 102 to correct the error before another wafer is processed. Additionally, the metrology station(s) 114 may also pass information to the metrology data analyzer 116 such that the process controller 110 for tool B 104 may be adjusted to compensate for the errors that were generated in tool A 102 and thus perform a feed-forward process for wafers that had already been processed incorrectly by tool A 102. In this manner, the invention provides an intra-tool monitoring and control system that can provide both feed-forward and feedback control of tools within a semiconductor wafer processing system.

[0016] The foregoing description describes the tools, processes controllers and

metrology stations as being separate physical elements. In practical systems, the tools may be integrated with the process controllers and one or more metrology stations may be integrated into one or more of the tools.

[0017] FIG. 2 depicts a flow diagram of an illustrative process 200 performed by the metrology station 114 and the metrology data analyzer 116. The process begins at step 202 when a wafer is received by a metrology station. At step 204, the method 200 queries whether the wafer requires metrology processing for patterned wafers or blanket wafers. A single wafer may have regions that are patterned and other regions that are blanket. As such, each region can be tested separately. If "patterned" is selected, the method proceeds to step 206 where one or more patterned wafer tests are selected to test the particular wafer. The selected patterned wafer test or tests depend on which tool processed the wafer in the last process step. At step 208, the selected patterned wafer test or tests are performed. If multiple tests are selected, each test is performed sequentially. Such patterned wafer testing includes:

1. Barrier seed step coverage of a trench and via having a specific size aspect ratio.
2. ECP gap fill based in a standard trench and via structure to detect voids.
3. ECP planarization in a particular trench/via structure.
4. CMP dishing and erosion in standard pattern structure (trenches with varying line width and spaces).
5. Copper thickness for various lines.
6. Trench depth after trench etch and dielectric constant after processing.
7. Residual metal on a comb structure.
8. Via or snake open in a standard structure - based on a voltage contrast or two-probe measurement.

[0018] If, at step 204, a blanket wafer is to be tested, then at step 210 the method 200 selects one or more blanket wafer tests. At step 212, the blanket wafer test(s) are performed. Blanket wafer tests include:

1. Barrier thickness.
2. Copper seed (CVD or PVD) thickness.

3. ECP copper thickness and bulk resistance.

4. Copper thickness.

5. Dielectric thickness, dielectric constant.

6. Defects such as particles, residue and systematic process defects.

[0019] Once the test results are produced, those test results are processed in step 214. At step 216, the method generates process control parameters for either feedback or feed-forward to the various process controllers. The process parameters may be changed to improve wafer processing. For example, in generating a barrier layer and a seed layer, the deposition process can be controlled by controlling power, pressure, bias, time of gas flows and the like to change the thickness or side wall coverage. In an electrochemical plating (ECP) gap fill process, the electroless thickness, patch thickness, current or pulse sequence, or additives to compensate for voids or planarization issues. In a chemical-mechanical polishing (CMP) process, the process can be controlled to minimize copper loss and achieve controlled thickness including controlling total pressure, radial pressure, slurry flow, rotation speed and time of CMP processing. Defects that are discovered in metrology testing can be controlled by eliminating some of the residue and particles produced in a prior process step by polishing or a longer cleaning period.

[0020] At step 218, the wafers removed from the metrology station and either discarded or moved to the next tool in the process sequence.

[0021] In one specific example, at step 202, each wafer is moved to a metrology station after ECP deposition of a copper layer. At steps 204, 210 and 212, the metrology station performs a blanket test to measure the thickness and uniformity of the copper layer. At step 214, the measurement results are processed to produce knowledge of the copper layer thickness a various locations on the wafer. At step 216, the process 200 generates control parameters for a CMP tool that will optimize the polishing of the copper layer with respect to the known thickness and uniformity. The control parameters include radial pressure profile (e.g., CMP pad pressure from center to edge) and the rotational speed of the polishing pad. At step 218, the polished wafer is moved to the next process tool.

[0022] FIG. 3 depicts a flow diagram of a method 300 representing a specific application of the invention in controlling the thickness of a copper interconnect. The process steps to be performed to produce a copper interconnect include etching a trench in the wafer (step 302), depositing a barrier layer of TaN and depositing a copper seed layer (step 304), depositing a copper layer (step 306) and then polishing the deposited copper back to the TaN (step 308) to form a copper interconnect in the trench.

[0023] After the barrier and seed layers are deposited, a metrology station measures the thickness of the layers at step 310. The results of the thickness measurements are used to produce control signals that are coupled to the deposition step 304 and the ECP step 306. In this manner, the barrier and seed layer deposition can be optimized for the next wafer and the ECP process can be used to compensate for anomalies in the seed layer thickness.

[0024] After ECP processing at step 306, the copper thickness and resistivity can be measured at step 312. The results are used to adjust the deposition step 304 and the ECP step 306 to correct any anomalies. The results are also used to control the CMP process 308. As such, if the copper thickness was not uniform after ECP step 306, the CMP step 308 can be used to correct the non-uniformity by adjusting the polishing rate, duration, slurry or other parameters.

[0025] Once the wafer exits the CMP step 308, metrology station measures the copper interconnect uniformity, residue remaining on the wafer and defects. The defects may be processed by a defect source identifier (as described in commonly assigned U.S. patent application 09/905,607, filed July 13, 2001, (Attorney Docket 4748 FET/MDR) or other know defect analysis system that can identify defect sources. This information is used to adjust the deposition step 304, the ECP step 306 and the CMP step 308 to optimize the processing of any new wafers as well as those in any intermediate step.

[0026] To further enhance the processing the deposition step 304 may be preceded by a metrology station measurement (step 316) that tests the geometry of the trench, e.g., depth, slope and the like. These measurements can be used to optimize any one or all of the following steps (e.g., steps 304, 306, and 308) in view of

the trench geometry.

[0027] While the foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.